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EXAMINER	
BOATENG, ALEXIS ASIEDUA	
ART UNIT	**PAPER NUMBER**
2838	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/700,812	MADER ET AL.	
	Examiner	Art Unit	
	Alexis Boateng	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,17,19,21-33,37,39,41 and 42* is/are rejected.

7)☒ Claim(s) *14-16,18,20,34-36,38 and 40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/16/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 4, 21, 22, 24, 41 and 42 are rejected under 35 U.S.C. 102 (b) as being anticipated by Darmawaskita (U.S. 6,184,659).

3. **Regarding claim 1**, Darmawaskita discloses a system for effectively managing operating power for an electronic device comprising:

a battery pack coupled to said electronic device for supplying said operating power to said electronic device (Figure 1, items 112 and 110; column 4 lines 56 through 59; A power converter 110 converts a power source (not illustrated) such as AC mains or a larger battery system such as found in an automobile to a voltage and current appropriate for charging a battery 112.)

a battery controller configured to alternately manage said battery pack in one of a single-cell implementation (Figure 1 item 112) and a dual-cell implementation (Figure 3 item 312a and 312b), said battery controller including a charge pump to provide an internal power supply for operating said battery controller in said single-cell implementation (column 5 lines 31 to 40; when the current and/or voltage inputs 116 are less than the set point(s) from the microprocessor 102, the SMPS controller 104 increases the pulse repetition rate and or duty cycle at the

output 114 which causes the power converter 110 to correspondingly increase the associated voltage and/or the current to the battery being charged).

Regarding claim 2, Darmawaskita discloses wherein said battery controller is implemented as a single-cell integrated circuit device that is selectively configurable to operate in either said single-cell implementation or said dual-cell implementation said battery pack (column 2 lines 10 through 12; Either the single or dual die implementations of the invention may be contained within a single integrated circuit package.).

Regarding claim 4, Darmawaskita discloses wherein said single-cell implementation of said battery pack utilizes a single lithium-ion battery cell, and wherein said dual-cell implementation of said battery pack utilizes two lithium-ion battery cells (column 12 lines 8 through 17; The SMPS controller 104 uses the CVCC (constant voltage with current compliance) mode to control in either the constant voltage or constant current mode. At the beginning of the Li-ion battery charging, the constant current mode is active. Once the battery voltage reaches its maximum voltage, the constant voltage mode will automatically take over, allowing the charger's firmware algorithm, since the SMPS controller 104 automatically takes care of the most critical step in the Li-ion battery charging process).

Regarding claim 21, Darmawaskita discloses a method for effectively managing operating power for an electronic device comprising the steps of:

Supplying said operating power for said electronic device from a battery pack coupled to said electric device; (Figure 1, items 112 and 110; column 4 lines 56 through 59; A power converter 110 converts a power source (not illustrated) such as AC mains or a larger battery system such as found in an automobile to a voltage and current appropriate for charging a battery 112.)

Managing said battery pack alternately in one of a single-cell implementation (Figure 1 item 112) and a dual-cell implementation (Figure 3 item 312a and 312b), by utilizing a battery controller that includes a charge pump to provide an internal power supply for operating said battery controller in said single-cell implementation (column 5 lines 31 to 40; when the current and/or voltage inputs 116 are less than the setpoint(s) from the microprocessor 102, the SMPS controller 104 increases the pulse repetition rate and or duty cycle at the output 114 which causes the power converter 110 to correspondingly increase the associated voltage and/or the current to the battery being charged).

Regarding claim 22, Darmawaskita discloses wherein said battery controller is implemented as a single integrated circuit device that is selectively configurable to operate in either said single – cell device or said dual-cell implementation of said battery pack (column 1 lines 6 - 7).

Regarding claim 24, Darmawaskita discloses wherein said single-cell implementation of said battery pack utilizes a single lithium-ion battery cell, and wherein said dual-cell implementation of said battery pack utilizes two lithium-ion battery cells (column 12 lines 8 through 17; The SMPS controller 104 uses the

CVCC (constant voltage with current compliance) mode to control in either the constant voltage or constant current mode. At the beginning of the Li-ion battery charging, the constant current mode is active. Once the battery voltage reaches its maximum voltage, the constant voltage mode will automatically take over, allowing the charger's firmware algorithm, since the SMPS controller 104 automatically takes care of the most critical step in the Li-ion battery charging process).

Regarding claim 41, Darmawaskita discloses a system for effectively managing operating power for an electronic device comprising:

a battery pack coupled to said electronic device for supplying said operating power to said electronic device (Figure 1, items 112 and 110; column 4 lines 56 through 59; A power converter 110 converts a power source (not illustrated) such as AC mains or a larger battery system such as found in an automobile to a voltage and current appropriate for charging a battery 112.) and

a battery controller configured to alternately manage said battery pack in one of a reduced-cell implementation (Figure 1 item 112) and an increased-cell implementation (Figure 3 item 312a and 312b), said battery controller including a charge pump to provide an internal power supply for operating said battery controller in said reduced-cell implementation (column 5 lines 31 to 40; when the current and/or voltage inputs 116 are less than the setpoint(s) from the microprocessor 102, the SMPS controller 104 increases the pulse repetition rate and or duty cycle at the output 114 which causes the power converter 110 to

correspondingly increase the associated voltage and/or the current to the battery being charged).

Regarding claim 42, Darmawaskita discloses a system for effectively managing operating power for an electronic device comprising:

means for supplying said operating power for said electronic device; (Figure 1, items 112 and 110; column 4 lines 56 through 59; A power converter 110 converts a power source (not illustrated) such as AC mains or a larger battery system such as found in an automobile to a voltage and current appropriate for charging a battery 112.) and

means for alternately managing said battery pack in one of a single-cell implementation (Figure 1 item 112) and a dual-cell implementation (Figure 3 item 312a and 312b), said means for managing including a charge pump to provide an internal controller power supply for operating said means for managing in said single – cell implementation (column 5 lines 31 to 40; when the current and/or voltage inputs 116 are less than the setpoint(s) from the microprocessor 102, the SMPS controller 104 increases the pulse repetition rate and or duty cycle at the output 114 which causes the power converter 110 to correspondingly increase the associated voltage and/or the current to the battery being charged).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 3 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Darmawaskita (U.S. 6,184,659) in view of Isono (U.S. 5,164,761)

Regarding claim 3, Darmawaskita discloses the claimed invention as defined in claim 1, but does not, expressly disclose the system wherein said electronic device is implemented as a portable electronic camera device that obtains said operating power from said battery pack, said battery controller providing remaining operating power information regarding said battery pack to said portable electronic camera device. Isono discloses in column 7 lines 6 to 14 wherein, when the battery pack is mounted on the camera body, the information stored in said information memory means and indicating the remaining capacity of the secondary battery is transmitted through said communicating means to said calculation means, and the information indicating the remaining capacity of the secondary battery, obtained in said calculation means, is transmitted through said communication means to said information memory means. At the time of invention, it would have been obvious to a person of ordinary skill in art to use Darmawaskita's battery system in the portable camera of Isono so as to provide

dual cell flexibility. It further would have been obvious to modify Darmawaskita's system and monitor battery status as taught by Isono so as to provide the user with an indication as to when the battery needs recharging or replacement.

Regarding claim 23, Darmawaskita discloses the claimed invention as defined in claim 21, but does not, expressly disclose the system wherein said electronic device is implemented as a portable electronic camera device that obtains said operating power from said battery pack, said battery controller providing remaining operating power information regarding said battery pack to said portable electronic camera device. Isono discloses in column 7 lines 6 to 14 wherein, when the battery pack is mounted on the camera body, the information stored in said information memory means and indicating the remaining capacity of the secondary battery is transmitted through said communicating means to said calculation means, and the information indicating the remaining capacity of the secondary battery, obtained in said calculation means, is transmitted through said communication means to said information memory means. At the time of invention, it would have been obvious to a person of ordinary skill in art to use Darmawaskita's battery system in the portable camera of Isono so as to provide dual cell flexibility. It further would have been obvious to modify Darmawaskita's system and monitor battery status as taught by Isono so as to provide the user with an indication as to when the battery needs recharging or replacement. Claim 5, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Darmawaskita (U.S. 6,184,659) in view of Dunsmore (U.S. 5,389,998)

Regarding claim 5, Darmawaskita discloses the claimed invention as defined in claim 1, but does not expressly disclose the system of claim 1 wherein said battery pack provides a reduced supply voltage to said battery controller in said single-cell implementation, said charge pump responsively increasing said reduced supply voltage in said single-cell implementation to thereby produce said internal controller power supply for powering said battery controller, said internal controller power supply thus being approximately equal in both said single-cell implementation and said dual-cell implementation, said charge pump selectably manipulating said reduced supply voltage by either a unity amplification factor, a 1.5 amplification factor, or times-two amplification factor, depending upon how much said reduced supply voltage needs to be increased to adequately provide said internal controller power supply. Dunsmore discloses in column 4 lines 48 through 55 that the controller 28 receives a signal from the shutter button 34 to end the reduced voltage mode of operation and restore normal operation of the boost circuit 30 and clock circuit. Dunsmore further discloses that the controller 28 activates the boost circuit 30 such that the boost circuit receives three - volt power from the power source 32 and boosts it to six-volt power. At the time of the invention, it would have been obvious to a person of ordinary skill of the art to construct the camera so that it boosts the voltage because, as stated in column 1 lines 30 through 33, that some of the camera systems can create momentarily large fluctuations in the demand for electrical power from the power supply system, which can reduce the available voltage. Therefore, as stated in column

1 lines 37 to 40, power systems include a boost circuit to amplify the reduced voltage.

Regarding claim 25, Darmawaskita discloses the claimed invention as defined in claim 21, but does not expressly disclose the system of claim 21 wherein said battery pack provides a reduced supply voltage to said battery controller in said single-cell implementation, said charge pump responsively increasing said reduced supply voltage in said single-cell implementation to thereby produce said internal controller power supply for powering said battery controller, said internal controller power supply thus being approximately equal in both said single-cell implementation and said dual-cell implementation, said charge pump selectably manipulating said reduced supply voltage by either a unity amplification factor, a 1.5 amplification factor, or times-two amplification factor, depending upon how much said reduced supply voltage needs to be increased to adequately provide said internal controller power supply. Dunsmore discloses in column 4 lines 48 through 55 that the controller 28 receives a signal from the shutter button 34 to end the reduced voltage mode of operation and restore normal operation of the boost circuit 30 and clock circuit. Dunsmore further discloses that the controller 28 activates the boost circuit 30 such that the boost circuit receives three - volt power from the power source 32 and boosts it to six-volt power. At the time of the invention, it would have been obvious to a person of ordinary skill of the art to construct the camera so that it boosts the voltage because, as stated in column 1 lines 30 through 33, that some of the camera systems can create momentarily

large fluctuations in the demand for electrical power from the power supply system, which can reduce the available voltage. Therefore, as stated in column 1 lines 37 to 40, power systems include a boost circuit to amplify the reduced voltage.

6. Claims 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Darmawaskita (U.S. 6,184,659) in view Sato (U.S. 5,985,480).

Regarding claim 6, Darmawaskita discloses the claimed invention as defined in claim 1, but does not expressly disclose the system wherein said battery pack has zero microamps of leakage current in a shutdown mode in which said battery pack has been discharged to a pre-determined threshold voltage level. Sato discloses in column 8 lines 4 through 10 that based on the level of at least 75% of the remaining capacity ration after being left as 45 C for a month of the single cells of the sealed alkaline storage battery of nickel-metal hydride system used in this experiment, it can be judged that entirely no leakage of current has taken place in the assembled batteries according to the present invention. At the time invention, it would have been obvious to a person of ordinary skill in the art to design the system where the battery pack has zero microamps of leakage current so that the battery's energy is not unnecessarily depleted during storage.

Regarding claim 26, Darmawaskita discloses the claimed invention as defined in claim 21, but does not expressly disclose the system wherein said battery pack has zero microamps of leakage current in a shutdown mode in which said battery pack has been discharged to a pre-determined threshold voltage level. Sato

discloses in column 8 lines 4 through 10 that based on the level of at least 75% of the remaining capacity ration after being left as 45 C for a month of the single cells of the sealed alkaline storage battery of nickel-metal hydride system used in this experiment, it can be judged that entirely no leakage of current has taken place in the assembled batteries according to the present invention. At the time invention, it would have been obvious to a person of ordinary skill in the art to design the system where the battery pack has zero microamps of leakage current so that the battery's energy is not unnecessarily depleted during shutdown or storage modes.

7. Claims 7, 8, 27, and 28 rejected under 35 U.S.C. 103(a) as being unpatentable over Darmawaskita (U.S. 6,184,659) in view of Hiratsuka (U.S. 5,680,027).

Regarding claim 7, Darmawaskita discloses the claimed invention as defined in claim 1, but does not, expressly disclose the system wherein said battery pack includes a charge switch and a discharge switch that are connected in a series configuration between a battery charger and one or more battery cells of said battery pack, said charge switch being opened by a CPU of said battery controller to prevent an overcharge condition in said battery cells. Hiratsuka discloses in column 4 lines 1 through 2 that the switch S1, which is turned on during the charging operation of the battery main unit and in column 4 lines 11 through 2 that the switch S2, which is turned on during the discharging of the

battery main unit. Hiratsuka further discloses in column 4 lines 43 through 47 the micro-computer 11, controlling the charging/discharging of the battery main unit 4 and the protective circuit inclusive of the analog circuit 12, has a plural input terminals, that is terminals controlling switches S1 to S4. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to allow the switches to be controlled by the CPU so that, as stated in column 5 lines 3 through 11, switches S1 or S2 are halted to prevent excessive charging or discharging.

Regarding claim 8, Darmawaskita discloses the claimed invention as defined in claim 1, but does not, expressly disclose the system wherein said battery pack includes a charge switch and a discharge switch that are connected in a series configuration between a battery charger and one or more battery cells of said battery pack, said discharge switch being opened by a CPU of said battery controller to prevent an overdischarge condition in said battery cells. Hiratsuka discloses in column 4 lines 1 through 2 that the switch S1, which is turned on during the charging operation of the battery main unit and in column 4 lines 11 through 2 that the switch S2, which is turned on during the discharging of the battery main unit. Hiratsuka further discloses in column 4 lines 43 through 47 the micro-computer 11, controlling the charging/discharging of the battery main unit 4 and the protective circuit inclusive of the analog circuit 12, has a plural input terminals, that is terminals controlling switches S1 to S4. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to

allow the switches to be controlled by the CPU so that, as stated in column 5 lines 3 through 11, switches S1 or S2 are halted to prevent excessive charging or discharging.

Regarding claim 27, Darmawaskita discloses the claimed invention as defined in claim 21, but does not, expressly disclose the method wherein said battery pack includes a charge switch and a discharge switch that are connected in a series configuration between a battery charger and one or more battery cells of said battery pack, said charge switch being opened by a CPU of said battery controller to prevent an overcharge condition in said battery cells. Hiratsuka discloses in column 4 lines 1 through 2 that the switch S1, which is turned on during the charging operation of the battery main unit and in column 4 lines 11 through 2 that the switch S2, which is turned on during the discharging of the battery main unit. Hiratsuka further discloses in column 4 lines 43 through 47 the micro-computer 11, controlling the charging/discharging of the battery main unit 4 and the protective circuit inclusive of the analog circuit 12, has a plural input terminals, that is terminals controlling switches S1 to S4. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to allow the switches to be controlled by the CPU so that, as stated in column 5 lines 3 through 11, switches S1 or S2 are halted to prevent excessive charging or discharging.

Regarding claim 28, Darmawaskita discloses the claimed invention as defined in claim 21, but does not, expressly disclose the method wherein said battery

pack includes a charge switch and a discharge switch that are connected in a series configuration between a battery charger and one or more battery cells of said battery pack, said discharge switch being opened by a CPU of said battery controller to prevent an overdischarge condition in said battery cells. Hiratsuka discloses in column 4 lines 1 through 2 that the switch S1, which is turned on during the charging operation of the battery main unit and in column 4 lines 11 through 2 that the switch S2, which is turned on during the discharging of the battery main unit. Hiratsuka further discloses in column 4 lines 43 through 47 the micro-computer 11, controlling the charging/discharging of the battery main unit 4 and the protective circuit inclusive of the analog circuit 12, has a plural input terminals, that is terminals controlling switches S1 to S4. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to allow the switches to be controlled by the CPU so that, as stated in column 5 lines 3 through 11, switches S1 or S2 are halted to prevent excessive charging or discharging.

8. Claim 9 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Darmawaskita (U.S. 6,184,659) in view of Sasaki (U.S. 6,335,611).

Regarding claim 9, Darmawaskita discloses the claimed invention as defined in claim 1, but does not expressly disclose wherein said battery pack includes a charge switch and a discharge switch that are connected in a series configuration between a battery charger and one or more battery cells of said battery pack, said battery controller including an internal negative charge pump that generates

a negative charge pump output voltage to a charge amplifier and a discharge amplifier that may then each generate a sufficient enhancement voltage to fully turn on a corresponding one of said charge switch and said discharge switch. Sasaki discloses in column 3, lines 33 to 34 that a switch 12 is used for conducting or interrupting a charging/discharging current route of the battery 13. Sasaki further discloses in column 3 lines 34 to 42 that when the comparator 17 (which is understood to be used as a form of a charge pump), has detected that a large charging current or a large discharging has exceeded a monitoring range, the controller 11 lower the amplification degree of the amplifier to make it possible to monitor a larger current than the monitoring range. When the comparator detects that a predetermined excess charging/discharging current is flowing, the controller 11 interrupts a discharging route of the switch 12. At the time of invention, it would have been obvious to a person of ordinary skill in the art to allow the battery controller to control the charge and discharge switches because, as stated in column 3 lines 47 through 51, the amplifier can detect a charging/discharging of a small current and when the comparator has detected an excess- charging or excess discharging current, the switch can protect the battery.

Regarding claim 29, Darmawaskita discloses the claimed invention as defined in claim 21, but does not expressly disclose wherein said battery pack includes a charge switch and a discharge switch that are connected in a series configuration between a battery charger and one or more battery cells of said battery pack,

said battery controller including an internal negative charge pump that generates a negative charge pump output voltage to a charge amplifier and a discharge amplifier that may then each generate a sufficient enhancement voltage to fully turn on a corresponding one of said charge switch and said discharge switch. Sasaki discloses in column 3, lines 33 to 34 that a switch 12 is used for conducting or interrupting a charging/discharging current route of the battery 13. Sasaki further discloses in column 3 lines 34 to 42 that when the comparator 17 (which is understood to be used as a form of a charge pump), has detected that a large charging current or a large discharging has exceeded a monitoring range, the controller 11 lower the amplification degree of the amplifier to make it possible to monitor a larger current than the monitoring range. When the comparator detects that a predetermined excess charging/discharging current is flowing, the controller 11 interrupts a discharging route of the switch 12. At the time of invention, it would have been obvious to a person of ordinary skill in the art to allow the battery controller to control the charge and discharge switches because, as stated in column 3 lines 47 through 51, the amplifier can detect a charging/discharging of a small current and when the comparator has detected an excess- charging or excess discharging current, the switch can protect the battery.

9. Claim 10 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Darmawaskita (U.S. 6,184,659) in view of Sasaki (U.S. 6,335,611), in view of Drake (U.S. 6,339,413).

Regarding claim 10, Darmawaskita and Sasaki discloses the system of claim 1 and the system of claim 9, but does not expressly disclose wherein said internal negative charge pump includes a first phase- 1 switch and a second phase-I switch that are closed to charge a capacitor with a charge pump output voltage from said charge pump, said internal negative charge pump subsequently closing a first phase- 0 switch and a second phase-o switch to provide said negative charge pump output voltage from said internal negative charge pump to both said charge amplifier and said discharge amplifier. Drake discloses in figure 5A switches that work in phases to charge capacitors from the charge pump output voltage. At the time of invention, it would have been obvious to a person of ordinary skill in the art have the charge pump include phase switches that close at different intervals of time so that, as recited by Drake in column 8 line 47, the desired voltage levels of the charge pump 75 are achieved.

Regarding claim 30, Darmawaskita and Sasaki discloses the method of claim 21 and the system of claim 29, but does not expressly disclose wherein said internal negative charge pump includes a first phase- 1 switch and a second phase-I switch that are closed to charge a capacitor with a charge pump output voltage from said charge pump, said internal negative charge pump subsequently closing a first phase- 0 switch and a second phase-o switch to

provide said negative charge pump output voltage from said internal negative charge pump to both said charge amplifier and said discharge amplifier. Drake discloses in figure 5A switches that work in phases to charge capacitors from the charge pump output voltage. At the time of invention, it would have been obvious to a person of ordinary skill in the art have the charge pump include phase switches that close at different intervals of time so that, as recited by Drake in column 8 line 47, the desired voltage levels of the charge pump 75 are achieved.

10. Claims 11, 12, 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Darmawaskita (U.S. 6,184,659) in view of Sakurai (U.S. 6,340,889).

Regarding claim 11, Darmawaskita discloses the claimed invention as defined in claim 1, but does not expressly disclose wherein said battery pack includes a charge switch and a discharge switch that are connected in a series configuration between a battery charger and one or more battery cells of said battery pack, said charge switch and said discharge switch being implemented as P-channel field-effect transistors that are located in a positive charge path between said battery charger and said one or more battery cells of said battery pack. Sakurai discloses in figure 1 items, 12 and 13 and in column 4 lines 3 through 8 that both of the switch devices 12 and 13 may instead be connected between the negative pole of the secondary battery 10 and the sense resistor 11. Sakurai further discloses that the kind (N-channel or P-channel) of switch device (e.g., the FET) would need to be suitably changed in correspondence to the circuit configuration.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to use a field effect transistor for the switch because it can switch signals of either polarity when necessary.

Regarding claim 12, Darmawaskita discloses the claimed invention as defined in claim 1, but does not expressly disclose wherein said battery pack includes a charge switch and a discharge switch that are connected in a series configuration between a battery charger and one or more battery cells of said battery pack, said charge switch and said discharge switch being implemented as N-channel field-effect transistors that are located in a positive charge path between said battery charger and said one or more battery cells of said battery pack. Sakurai discloses in figure 1 items, 12 and 13 and in column 4 lines 3 through 8 that both of the switch devices 12 and 13 may instead be connected between the negative pole of the secondary battery 10 and the sense resistor 11. Sakurai further discloses that the kind (N-channel or P-channel) of switch device (e.g., the FET) would need to be suitably changed in correspondence to the circuit configuration. At the time of invention, it would have been obvious to a person of ordinary skill in the art to use a field effect transistor for the switch because it can switch signals of either polarity when necessary.

Regarding claim 31, Darmawaskita discloses the claimed invention as defined in claim 21, but does not expressly disclose wherein said battery pack includes a charge switch and a discharge switch that are connected in a series configuration between a battery charger and one or more battery cells of said battery pack,

said charge switch and said discharge switch being implemented as P-channel field-effect transistors that are located in a positive charge path between said battery charger and said one or more battery cells of said battery pack. Sakurai discloses in figure 1 items, 12 and 13 and in column 4 lines 3 through 8 that both of the switch devices 12 and 13 may instead be connected between the negative pole of the secondary battery 10 and the sense resistor 11. Sakurai further discloses that the kind (N-channel or P-channel) of switch device (e.g., the FET) would need to be suitably changed in correspondence to the circuit configuration. At the time of invention, it would have been obvious to a person of ordinary skill in the art to use a field effect transistor for the switch because it can switch signals of either polarity when necessary.

Regarding claim 32, Darmawaskita discloses the claimed invention as defined in claim 21, but does not expressly disclose wherein said battery pack includes a charge switch and a discharge switch that are connected in a series configuration between a battery charger and one or more battery cells of said battery pack, said charge switch and said discharge switch being implemented as N-channel field-effect transistors that are located in a positive charge path between said battery charger and said one or more battery cells of said battery pack. Sakurai discloses in figure 1 items, 12 and 13 and in column 4 lines 3 through 8 that both of the switch devices 12 and 13 may instead be connected between the negative pole of the secondary battery 10 and the sense resistor 11. Sakurai further discloses that the kind (N-channel or P-channel) of switch device (e.g., the FET)

would need to be suitably changed in correspondence to the circuit configuration. At the time of invention, it would have been obvious to a person of ordinary skill in the art to use a field effect transistor for the switch because it can switch signals of either polarity when necessary.

11. Claims 13, 17, 33, and 37 rejected under 35 U.S.C. 103(a) as being unpatentable over Darmawaskita (U.S. 6,184,659) in view of Piercey (U.S. 5,557,188).

Regarding claim 13, Darmawaskita discloses the claimed invention as defined in claim 1, but does not expressly disclose wherein said battery pack is implemented in said single-cell implementation, said battery controller coordinating a startup procedure for said battery pack during which a battery charger is connected to said battery pack in a discharged state, said battery controller responsively closing a charge switch that is coupled between said battery charger and a battery cell of said battery pack. Piercey discloses in column 8 lines 23 through 27 that the battery controller 355 automatically turns on transistor 382 and thus reconnects battery 353 to terminal 351 once the input charge voltage is within the acceptable operating range, and the battery system is reset upon receipt of a BATTIN signal from an external system. The transistor is understood as a charge switch that is turned on by battery controller and is coupled between the battery charger and battery cell. At the time of invention, it would have been obvious to someone of ordinary skill in the art to have the

battery controller close the charge switch to monitor the discharge and prevent overdischarge.

Regarding claim 17, Darmawaskita discloses the claimed invention as defined in claim 1, but does not expressly disclose wherein an analog-to-digital converter module of said battery controller monitors a battery voltage of said battery pack as it discharges while supplying said operating power to said electronic device, a CPU of said battery controller controlling a shutdown procedure for said battery pack when a pre-determined discharged voltage level is sensed by said analog-to-digital converter module, said CPU responsively opening a discharge switch in said battery pack. Piercey discloses in column 5, lines 46 through 51 that the voltage of battery 353 is also applied to an analog-to-digital converter input lead of battery controller 355, thereby allowing digital processing of the charge/discharge current of battery 353 as measured by the voltage across resistive device 359, and digital processing of voltage battery 353. Piercey further discloses in column 7, lines 38 to 41 that the discharge of battery 351 at voltages below cutoff is preferably not allowed in order to avoid battery degradation and to achieve maximum battery life and charge/discharge cycles. He further discloses in column 7 lines 47 to 53 that the battery controller 355 is able to determine the charge state of battery 353 by monitoring the voltage of battery 353 and the charge current over time, in order to determine when battery 353 has reached such usable recharge level prior to allowing transistors 381 and 382 to conduct current from battery 353 to power a system. At the time of

invention, it would have been obvious to someone skilled in the art that using and analog to digital converter for an input lead of the battery controller because it allows an efficient digital processing of the charge/discharge current of the battery as stated in column 5 lines 48- 49.

Regarding claim 33, Darmawaskita discloses the claimed invention as defined in claim 21, but does not expressly disclose wherein said battery pack is implemented in said single-cell implementation, said battery controller coordinating a startup procedure for said battery pack during which a battery charger is connected to said battery pack in a discharged state, said battery controller responsively closing a charge switch that is coupled between said battery charger and a battery cell of said battery pack. Piercey discloses in column 8 lines 23 through 27 that the battery controller 355 automatically turns on transistor 382 and thus reconnects battery 353 to terminal 351 once the input charge voltage is within the acceptable operating range, and the battery system is reset upon receipt of a BATTIN signal from an external system. The transistor is understood as a charge switch that is turned on by battery controller and is coupled between the battery charger and battery cell. At the time of invention, it would have been obvious to someone of ordinary skill in the art to have the battery controller close the charge switch to monitor the discharge and prevent overdischarge.

Regarding claim 37, Darmawaskita discloses the claimed invention as defined in claim 21, but does not expressly disclose wherein an analog-to-digital

converter module of said battery controller monitors a battery voltage of said battery pack as it discharges while supplying said operating power to said electronic device, a CPU of said battery controller controlling a shutdown procedure for said battery pack when a pre-determined discharged voltage level is sensed by said analog-to-digital converter module, said CPU responsively opening a discharge switch in said battery pack. Piercey discloses in column 5, lines 46 through 51 that the voltage of battery 353 is also applied to an analog-to-digital converter input lead of battery controller 355, thereby allowing digital processing of the charge/discharge current of battery 353 as measured by the voltage across resistive device 359, and digital processing of voltage battery 353. Piercey further discloses in column 7, lines 38 to 41 that the discharge of battery 351 at voltages below cutoff is preferably not allowed in order to avoid battery degradation and to achieve maximum battery life and charge/discharge cycles. He further discloses in column 7 lines 47 to 53 that the battery controller 355 is able to determine the charge state of battery 353 by monitoring the voltage of battery 353 and the charge current over time, in order to determine when battery 353 has reached such usable recharge level prior to allowing transistors 381 and 382 to conduct current from battery 353 to power a system. At the time of invention, it would have been obvious to someone skilled in the art that using and analog to digital converter for an input lead of the battery controller because it allows an efficient digital processing of the charge/discharge current of the battery as stated in column 5 lines 48- 49.

12. Claims 19 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Darmawaskita (U.S. 6,184,659) in view of Nelson et al. (U.S. 6,098,095)

Regarding claim 19, Darmawaskita discloses the claimed invention as defined in claim 1, but does not expressly disclose wherein said battery controller includes a UART device that is implemented to communicate with said electronic device via a single transmit/receive pin on an integrated circuit device that contains said battery controller, said UART thus supporting a single-pin UART interface to conserve available connection pins on said integrated circuit device of said battery controller. Nelson discloses in column 4 lines 10 through 14 that for effective communication, both microprocessors 12 and 32 must be equipped with compatible communication software and appropriate hardware as needed to enable communication over a single I/O path. Nelson further discloses in column 4 lines 18 through 21 that a UART system can be implemented by the use of stand alone parts and rely only on a single I/O pin. At the time of invention it would have been obvious to someone skilled in the art that using a UART device is more beneficial because, as stated in column 1 lines 61 through 64, they can mate and work effectively with their single-signal, single axis counterparts, an thereby provide "backward compatibility."

Regarding claim 39, Darmawaskita discloses the claimed invention as defined in claim 21, but does not expressly disclose wherein said battery controller includes a UART device that is implemented to communicate with said electronic

device via a single transmit/receive pin on an integrated circuit device that contains said battery controller, said UART thus supporting a single-pin UART interface to conserve available connection pins on said integrated circuit device of said battery controller. Nelson discloses in column 4 lines 10 through 14 that for effective communication, both microprocessors 12 and 32 must be equipped with compatible communication software and appropriate hardware as needed to enable communication over a single I/O path. Nelson further discloses in column 4 lines 18 through 21 that a UART system can be implemented by the use of stand alone parts and rely only on a single I/O pin. At the time of invention it would have been obvious to someone skilled in the art that using a UART device is more beneficial because, as stated in column 1 lines 61 through 64, they can mate and work effectively with their single-signal, single axis counterparts, an thereby provide "backward compatibility."

Allowable Subject Matter

13. Claims 14 – 16, 18, 20, 34-36, 38, and 40 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 14 recites, inter alia, a system as defined in claim 13, wherein said charge pump responsively generating a charge pump output voltage at a pre-determined voltage level to a charger regulator that filters said charge pump output voltage, said charger regulator then generating said internal controller power supply so

that a CPU of said battery controller may begin executing battery controller instruction to control operations of said battery pack.

Claim 15 recites, inter alia, a system as defined in claim 14, wherein said CPU also utilizing a CPSEL line to switch from said charger input of said charge pump to a battery input of said charge pump, said charge pump thus compensating for a reduced battery output voltage resulting from said single-cell implementation for said battery pack.

Claim 16 recites, inter alia, a system as defined in claim 15 wherein said battery pack utilizes said battery charger under control of said battery controller to charge said battery cell, said battery charger being subsequently disconnected for a more unrestricted use of said electronic device utilizing said battery pack to supply to said operating power.

Claim 18 recites, inter alia, a system as defined in claim 17 wherein CPU toggles a CPSEL line switch from a battery voltage of said battery pack at a battery input of said charge pump to charge voltage from said battery charger at a charger input of said charge pump to thereby generate said internal controller power supply.

Claim 20 recites, inter alia a system as defined in claim 19 where in said UART device receives a timebase signal from a precision instruction oscillator that is implemented on an integrated circuit that includes said battery controller, said instruction oscillator accurately generating a UART clock signal to said UART for synchronizing UART operations.

Claim 34 recites, inter alia, a system as defined in claim 33, wherein said charge pump responsively generating a charge pump output voltage at a pre-determined voltage level to a charger regulator that filters said charge pump output voltage, said charger regulator then generating said internal controller power supply so that a CPU of said battery controller may begin executing battery controller instruction to control operations of said battery pack.

Claim 35 recites, inter alia, a system as defined in claim 34, wherein said CPU also utilizing a CPSEL line to switch from said charger input of said charge pump to a battery input of said charge pump, said charge pump thus compensating for a reduced battery output voltage resulting from said single-cell implementation for said battery pack.

Claim 36 recites, inter alia, a system as defined in claim 35 wherein said battery pack utilizes said battery charger under control of said battery controller to charge said battery cell, said battery charger being subsequently disconnected for a more unrestricted use of said electronic device utilizing said battery pack to supply to said operating power.

Claim 38 recites, inter alia, a system as defined in claim 37 wherein CPU toggles a CPSEL line switch from a battery voltage of said battery pack at a battery input of said charge pump to charge voltage from said battery charger at a charger input of said charge pump to thereby generate said internal controller power supply.

Claim 40 recites, inter alia a system as defined in claim 39 where in said UART device receives a timebase signal from a precision instruction oscillator that is implemented on an integrated circuit that includes said battery controller, said instruction oscillator accurately generating a UART clock signal to said UART for synchronizing UART operations.

The art of record does not disclose the above limitations, nor would it be obvious to modify it in such a manner.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kawamura (U.S. 5,784,105) teaches a video camera with a built-in secondary battery with a terminal used for connection with an external power source. The video camera is arranged in such that the circuit part is connected to the built – in secondary battery or to the external power source when the main switch is closed and that the built in secondary battery can be connected to the external power source when the main switch is open (see Figures 1 and 2; Abstract lines 1 through 2 and 5 through 10).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexis Boateng whose telephone number is (571) 272-5979. The examiner can normally be reached on 8:30 am - 6:00 pm, Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Sherry can be reached on (571) 272-2084. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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AB

6/23/05

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